REMARKS

In the Office Action, claims 41-45 and 47-48 are rejected under 35 U.S.C. §103(a) as being unpatentable over Lin and Akram et al. in view of Rostoker et al. Claims 49-54 and 56-57 are rejected under 35 U.S.C. §103(a) as being unpatentable over Tanioka in view of Rostoker et al. Applicants respectfully contend that the instant invention is patentable over the cited prior arts and the reasons are discussed in the following.

Rejection of claims 41-45 and 47-48 under 35 U.S.C. §103(a)

Lin discloses a multi-chip module board on which a plurality of individually packaged chip packages are mounted (col. 1, lines 38-40 and FIG. 1A). As can be seen from FIG. 1A, the multi-chip module board is a circuit board that has no connection to other circuit board and is not meant to be further enclosed or packaged. **Nowhere has Lin's disclosure motivated a person skilled in the art to further enclose or package a multi-chip substrate and individually packaged chip packages** as claimed in claim 41 because Lin's art is not intended to be further packaged.

Akram et al. teach a semiconductor package comprising multiple stacked substrates having flip chips attached to the substrates with chip on board assembly technique to achieve dense packaging. The key subject matter in the art of Akram et al. is to stack multiple substrates of bare chips in the vertical direction to achieve high density. Akram et al. also teach that **an encapsulation material may cover the stack dice portion** of the stacked assembly (col. 6, lines 61-62). It is clear that the teaching is to cover the "dice portion". There is absolutely no teaching or suggestion to enclose or

package **a multi-chip substrate and individually packaged chip packages** as claimed in claim 41.

Rostoker et al. disclose a technique for individually electronically selecting unsingulated dies on a wafer for testing. The disclosed art does not teach or suggest any multi-chip module packaging. Applicants also like to point out that the art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** in the semiconductor industry. As recited in claim 41, "**said at least two chip packages having been burn-in tested and function tested**" is the subject matter of this invention that is very different from the teaching of Rostoker et al.

As pointed out in the specification of the instant invention and previous amendments, the gist of this invention is to **package a multi-chip module that encloses individually packaged chips into a ball grid array package**, and hence the package structure of the invention as recited in claim 41 is invented.

From the above discussion, it is evident that none of the cited prior arts disclose or suggest **packaging a multi-chip substrate and individually packaged chip packages that are burn-in tested and function tested** of claim 41. Furthermore, neither Lin nor Akram et al. suggest packaging the multi-chip module into a **ball grid array package**. Applicants respectfully submit that claim 41 in its amended form has overcome the rejection under U.S.C. §103(a) over Lin and Akram et al. in view of Rostoker et al. Claims 41-45 and 47-48 should be allowable.

Rejection of claims 49-54 and 56-57 under 35 U.S.C. §103(a)

Tanioka teaches a thin multi-layer board 11 formed on a thick multi-layer board 10 and a multi-layer hybrid circuit formed by the wire-bonding of "bare chips" and the mounting of chip parts (col. 1, lines 39-47). Tanioka **does not teach any chip package being a packaged chip module having a bare chip and a chip substrate packaged and enclosed therein, said at least one chip package having been burn-in tested and function tested**. The bare chip 2 and the multi-layer board 11 are encapsulated while they are mounted on the multi-layer board 10. It is not a chip package having been packaged and burn-in tested in the package.

As discussed earlier, Rostoker et al. does not teach or suggest any multi-chip module packaging. The art of Rostoker et al. is for **testing unsingulated dies** on a wafer that is completely different from the art of **testing a chip scale package** which is done after the dies have been cut, separated and packaged in the semiconductor industry. As recited in claim 49, "**said at least one chip package having been burn-in tested and function tested**" is the subject matter of this invention that is very different from the teaching of Rostoker et al.

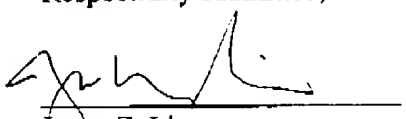
From FIG. 1 of Tanioka's art, it can be seen that the bare chip 2 and thin multi-layer board 11 are encapsulated directly above the multi-layer board 10 and the encapsulation material also covers the multi-layer board 10. **There does not exist any chip package being a packaged chip module which has been burn-in tested and function tested.** Consequently, the combination of Rostoker et al. and Tanioka can not reach the subject matter of claim 49 that recites "**at least one chip packaging having**

been burn-in tested and function tested".

From the above discussion, it is evident that none of the cited prior arts discloses or suggests **packaging a multi-chip substrate and individually packaged chip packages that are burn-in tested and function tested** of claim 49. Furthermore, Tanioka does not suggest packaging the multi-chip module into a **ball grid array package**. Applicants respectfully submit that claim 49 in its amended form has overcome the rejection under U.S.C. §103(a) over Tanioka in view of Rostoker et al. Claim 50 has been amended to correct the error pointed out by the examiner. Claims 49-54 and 56-57 should be allowable.

In summary, from the foregoing discussion it is clear that the instant invention differs from the cited prior arts. The physical difference results in different effects and is not obvious. The amended base claims 41 and 49 have clearly defined the unique feature of this invention and overcome all the rejections under 35 U.S.C. §103(a) and should be patentable. By virtue of dependency, claims 42-45, 47-48 and 50-54, 56-57 should also be patentable. **A Credit Card Payment Form PTO-2038 in the amount of $750.00 is submitted to cover the Large Entity RCE fee.** Prompt and favorable reconsideration of the application is respectfully solicited.

Respectfully submitted,



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